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In yet another aspect, the present invention provides a method for transferring data between a CPU and a plurality of coprocessors. The method includes transmitting instructions to the plurality coprocessors, each of the instructions directing a data transfer between the CPU and a specific coprocessor, where the transmitting is provided in a specific instruction order; and subsequently transferring the data in an order different from the specific instruction order. The transferring includes prescribing transfer of a data element corresponding to a specific outstanding instruction relative to all outstanding instructions, the outstanding instructions being those instructions that have not completed a subsequent data transfer.

Other features and advantages of the present invention will become apparent upon study of the remaining portions of the specification and drawings.

Kindly amend the section entitled ABSTRACT OF THE DISCLOSURE as follows:

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ABSTRACT OF THE DISCLOSURE

An interface for transferring data between a central processing unit (CPU) and a plurality of coprocessors is provided. The interface includes an instruction bus and a data bus. The instruction bus is configured to transfer instructions to the plurality of coprocessors in an instruction transfer order, where particular instructions direct designated ones of the plurality of coprocessors to transfer the data to/from the CPU. The data bus is configured to subsequently transfer the data. Data order signals within the data bus prescribe a data transfer order that differs from the instruction transfer order by prescribing a transfer corresponding to a specific outstanding particular instruction relative to all outstanding particular instructions.